Mengyuan YIN

+44 7521165341 • mengyuan.yin20@imperial.ac.uk • Mengyuan410 (github.com)

EDUCATION

Imperial College London, United Kingdom

10/2020 - Present

- Master of Engineering (MEng) in Electronic and Information Engineering
- Average Score:

87.30% (Year 1): Head of Department's Prize for Top Student in First Year 82.86% (Year 2): Top 5%

PROFESSIONAL EXPERIENCE

Institute of Computing Technology Chinese Academy of Science

04/2023 - Present

Research Internship, Research Group: Dr. Kan Shi

- Developed a hardware fuzzing system to verify RISC-V processors by automatically generating stimuli.
- Implemented the hardware fuzzing system on Sidewinder-100 SoC.

Imperial College London, London, United Kingdom

07/2022 - 09/2022

Undergraduate Research Opportunity Programme, Research Group: Prof. Timothy Constandinou

- Analysed signals recorded by an IR-UWB radar system for human behavioural monitoring.
- Utilised different filtering techniques to extract human respirational signals from clutters and signals caused by the dynamic motions of a rotating rigid body such as a fan.

Agency for Science, Technology and Research (A*STAR), Singapore

07/2021 - 09/2021

Research Assistant, Research Group: Dr. Yuan GAO

- Built a Long Short-Term Memory model to predict different types of heart conduction abnormalities.
- Tested the performance of the model for both floating-point and fixed-point data type, for the possible future implementation of the model on hardware.

HIGHLIGHTED PROJECTS

The Mars Rover Project

05/2022 - 06/2022

- Built an autonomous rover system with an ESP32 which can navigate through an arena, detect obstacles, and map its routine and detection on a developed web app.
- Mainly responsible for data management and the communication among the ESP32, a DynamoDB cloud database, and the web app. Developed the web app with React and Node.js.
- Selected as the runner up for the second-year Mars Rover Group Project amidst the cohort.

The FPGA IoT Project

02/2022 - 03/2022

 Developed an IoT multi-player gaming system with each node consisting of an FPGA acting as the gaming controller and a game host on the computer. Data synchronisation among nodes is facilitated by the AWS cloud server using UDP protocol.

The C-to-MIPS Compiler Project

02/2022 - 03/2022

- Used Flex to lex, Yacc to parse, and C++ to generate MIPS code from input ANSI C programmes.
- Passed 91% of the examiner's tests ranked second of the cohort.

The MIPS-CPU Project

11/2021 - 12/2021

- Used Verilog to develop both a pipelined and non-pipelined version of MIPS-compatible CPU, which interacts with the memory with a single Avalon compatible memory-mapped interface.
- Created a robust testbench including a virtual RAM memory, a random MIPS-code generator and a reference CPU programmed using C++.

The Circuit Simulator Project

05/2021 - 06/2021

- Programmed a circuit simulator with C++ which reads the component netlist of a circuit and produces magnitude and phase response through AC and DC analysis
- Selected as the best first-year Circuit Simulator Group Project amidst the cohort